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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,372	04/30/2004	Ko-Hsing Chang	12409-US-PA	3371

31561 7590 05/20/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER

TRAN, MAI HUONG C

ART UNIT	PAPER NUMBER
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2818

DATE MAILED: 05/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.		Applicant(s)	
	10/709,372		CHANG ET AL.	
	Examiner		Art Unit	
	Mai-Huong Tran		2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 May 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-6 and 9-10 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,486,028 to Chang et al. in view of Fastow et al. (6,583,479).

Regarding to claim 1, Chang discloses a non-volatile memory cell comprising a substrate 100, having a trench 102 thereon; a gate 116, formed within the trench 102; a first source/drain region 108, formed at a bottom of the trench 102; a composite dielectric layer 110, 112, 114, formed between the gate 116 and a surface of the trench (fig. 5), wherein the composite dielectric layer comprises at least a charge-trapping layer 112; and a second source/drain region 104, 106, formed in the substrate 100 on each side of the gate 116 (col. 3, lines 13-63, and fig. 6). Chang does not disclose the amended claim 1 with a third source/drain region located in the substrate on the other side of the gate,

wherein the second source/drain region and the third source/drain region are electrically connected to a common bit line.

However, Fastow teaches a third source/drain region located in the substrate on the other side of the gate, wherein the second source/drain region and the third source/drain region are electrically connected to a common bit line (fig. 10).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a third source/drain region located in the substrate on the other side of the gate, wherein the second source/drain region and the third source/drain region are electrically connected to a common bit line, as taught by Fastow in order to grow for higher density devices capable of storing more and more information in a smaller package, there becomes a need to pack more and more memory cells into these memory arrays. Further, these memory arrays must be made as small as possible (col. 13, lines 38-42).

Regarding to claim 2, Chang discloses the non-volatile memory cell wherein the gate 116 completely fills the trench 102 (fig. 6).

Regarding to claim 3, Chang discloses the non-volatile memory cell wherein the gate fills the trench the trench and protrudes above the substrate surface (fig. 6).

Regarding to claim 4, Chang discloses the non-volatile memory cell wherein the gate further laterally extend above the substrate outside the trench (fig. 6).

Regarding to claim 5, the non-volatile memory cell wherein the composite dielectric layer also laterally extend above the substrate outside the trench and positioned between the gate and the substrate (fig. 6).

Regarding to claim 6, Chang discloses the non-volatile memory cell wherein the composite dielectric layer further comprises a bottom oxide layer 110, wherein the charge-trapping layer 112 located between the gate 116 and the bottom oxide layer 110; and a cap oxide layer 114, located between the gate 116 and the charge-trapping layer 112 (fig. 6).

Regarding to claim 9, Chang discloses the non-volatile memory cell wherein material constituting the gate comprises polysilicon (col. 4, lines 22-24).

Regarding to claim 10, Chang discloses the non-volatile memory cell wherein the composite dielectric layer comprises a silicon oxide/silicon nitride/silicon oxide layer (col. 3, lines 53-56, fig. 6).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 7 and 8 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,486,028 to Chang in view of Fastow et al. (6,583,479) and further in view of Forbes (US pub. No. 2003/0235076).

Regarding to claim 7, Chang in view of Fastow discloses the claimed invention except for the non-volatile memory cell further comprising spacers formed on the sidewalls of the gate. Forbes teaches the non-volatile memory cell further comprising spacers formed on the sidewalls of the gate (page 6, [0058], and fig. 7A).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the non-volatile memory cell further comprising spacers formed on the sidewalls of the gate, as taught by Forbes in order to improve a multistate NROM operate with lower programming voltages than that used by conventional DRAM cells, yet still hold sufficient charge to withstand the effects of parasitic capacitances and noise due to circuit operation.

Regarding to claim 8, Forbes discloses the non-volatile memory cell further comprising a lightly doped region formed in the substrate underneath the spacers (page 7, [0060], and figs. 7A, 7B).

Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

Applicants argue that Chang fails to teach or disclose the emphasized features in the amended independent claim 1, "the second source/drain region and the third source/drain region are electrically connected to a common bit line". However, "the second source/drain region and the third source/drain region are electrically connected to a common bit line" was well known in the art. For example, fig. 10 of Fastow et al., in view of the new ground of rejection, discloses "the second source/drain region and the third source/drain region are electrically connected to a common bit line". For the above reasons, it is believed that the rejections should be sustained. Feature of an invention not found in the claims can be given no patentable weight in distinguishing the claimed invention over the prior art.

Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP 706.07(a). Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for response to this final action is set to expire THREE MONTHS from the date of this action. In the event a first response is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for response expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (571) 272-1796. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (571) 272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.


Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you

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have questions on access to the Private PAIR system, contact the Electronic Business

Center (EBC) at 866-217-9197 (toll-free).


Mai-Huong Tran


David Nelms
Supervisory Patent Examiner
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